REMARKS

The paper is in response to the Office Action mailed March 19, 2010 ("the Office Action"). The foregoing amendment cancels claims 2, 10-12, and 15-17; amends claims 1, 3, 6, 7, 9, 13, and 14; and adds new claims 30. Claims 1, 3, 4, 6-9, 13, 14, 18-24, and 26-30 are now pending in view of the amendments. Applicants respectfully request reconsideration of the application in view of the above amendments to the claims and the following remarks. For Examiner's convenience and reference, Applicants present remarks in the order that the Office Action raises the corresponding issues.

In connection with the prosecution of this case and any related cases, Applicants have, and/or may, discuss various aspects of the disclosure of the cited references as those references are then understood by the Applicants. Because such discussion could reflect an incomplete or incorrect understanding of one or more of the references, the position of the Applicants with respect to a reference is not necessarily fixed or irrevocable. Applicants thus hereby reserve the right, both during and after prosecution of this case, to modify the views expressed with regard to any reference.

Please note that Applicants do not intend the following remarks to be an exhaustive enumeration of the distinctions between any cited references and the claims. Rather, Applicants present the distinctions below solely by way of example to illustrate some of the differences between the claims and the cited references. Finally, Applicants request that Examiner carefully review any references discussed below to ensure that Applicants' understanding and discussion of any reference is consistent with Examiner's understanding.

Unless otherwise explicitly stated, the term "Applicants" is used herein generically and may refer to a single inventor, a set of inventors, an appropriate assignee, or any other entity or person with authority to prosecute this application.

I. Rejection under 35 U.S.C §103(a)

The Office action rejects the claims under 35 U.S.C §103(a) as follows:

- Claims 1-3, 6-7, 9-12, 19-20, 24-26, 28, and 29 are rejected as being unpatentable over *Khoury, Jr. et al.* (U.S. Patent Publication No. 2004/0042504) in view of *Lutz* (U.S. Patent No. 4,276,548);

- Claims 14-16, and 27 are rejected as being unpatentable over what the Examiner characterizes as "admitted prior art" ("*APA*") in view of *Lutz*;

- Claim 4 is rejected as being unpatentable over *Khoury* in view of *Lutz* as applied to claim 1, and further in view of "Transistors" at www.electronics-tutorials.com ("*Transistors Tutorial*");

- Claim 21 is rejected as being unpatentable over *Khoury* in view of *Lutz* as applied to claim 19, in further view of *Transistors Tutorial*;

- Claim 26 is rejected as being unpatentable over *Khoury* in view of *Lutz*;

- Claim 17 is rejected as being unpatentable over *APA* in view of *Lutz* as applied to claim 14, in further view of *Rumbaugh* (U.S. Patent No. 6,275,144);

- Claim 8 is rejected as being unpatentable over *Khourdy* in view of *Lutz* as applied to claim 7, and further in view of "Phase-Locked Loop Protocol Scheme for a Synchronization Field," IBM Technical Disclosure Bulletin, May 1990 ("*IBM TDB*");

- Claims 13, 22, and 23 are rejected as being unpatentable over *Khoury* in view of *Lutz* as applied to claims 12, 19, respectively, and further in view of *IBM TBD*; and

- Claim 18 is rejected as being unpatentable over *APA* in view of *Lutz* as applied to claim 14, respectively, and further in view of *IBM TBD*.

Applicants respectfully traverse the rejection.

Under 35 U.S.C §103(a), "[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." According to MPEP §2142, "[t]he examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." Finally, MPEP 2141.III notes that:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Court quoting *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), stated that "'[R]ejections on obviousness cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.'" *KSR*, 550 U.S. at ___, 82 USPQ2d at 1396.

A. Independent Claim 1

Claim 1, as amended, recites a fiber-optic transducer that produces a lock signal only when data is present in a serial data signal, as indicated by a synchronization signal, the transponder comprising, among other things: "a timing circuit…including a comparator that compares a first reference signal with a signal from the capacitor and resistor network used to measure the period of time that the synchronization signal is asserted, the comparator outputting the lock signal based on the comparison." Figure 2 of Applicants' specification (copied below) illustrates an example embodiment of the claimed timing circuit (12) including a comparator (46) that compares a first reference signal (V_{REF}) with a signal from a capacitor (44) and resistor (R4) network.

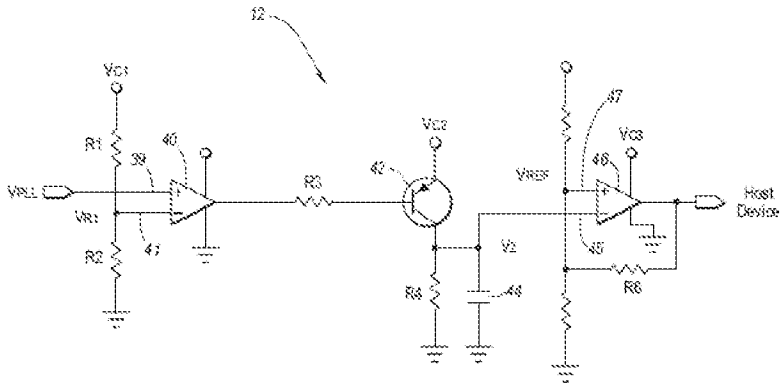
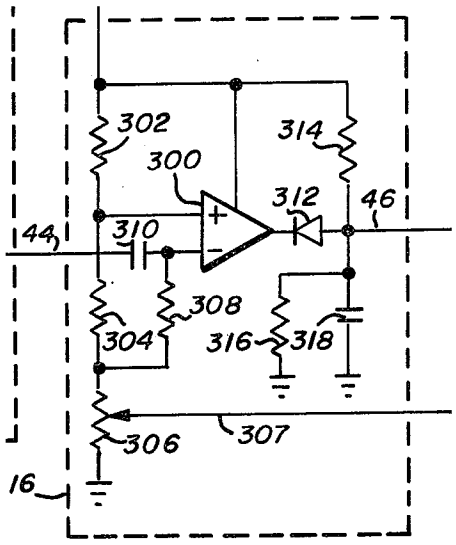


Fig. 2

In rejecting claim 1, the Examiner relies on *Khoury* as purportedly teaching a demultiplexer, but concedes that *Khoury* "fails to disclose the limitations of the PLL." *See Office Action* at 3. The Examiner instead cites *Lutz* for its purported teaching of a PLL and a timing circuit. *See id.* However, as explained below, the "timing circuit" of *Lutz* does not include "a comparator that compares a first reference signal with a signal from [a] capacitor and resistor network used to measure the period of time that [a] synchronization signal is asserted," as presently claimed.

The Examiner characterizes lock detector and timer (16) of *Lutz* as corresponding to the claimed "timing circuit" and characterizes an operational amplifier (300) in lock detector and timer (16) as corresponding to the claimed "comparator." *See Office Action* at 4 and 5. According to *Lutz*, lock detector and timer (16) outputs a "stabilization signal" a predetermined period after a lock signal output by a PLL (14) has stabilized. *See Lutz*, col. 3, lines 56-59. Details of *Lutz's* lock detector and timer (16) are illustrated in the excerpted portion of Figure 3A of *Lutz* copied below.



Lutz's amplifier (300) produces the stabilization signal by comparing the PLL lock signal on line (44) (applied to its inverting input, as shown above) with a "reference potential" (applied to its non-inverting input). *See Lutz* at col. 7, line 56, through col. 8, line 22. However, the PLL lock signal (44) input to amplifier (300) is not from a "capacitor and resistor network" that is used to "measure a period of time that a synchronization signal is asserted," as claimed. This distinction is illustrated by comparing the figures copied above. As shown in *Lutz* Figure 3A, the signal fed to the non-inverting input of *Lutz's* amplifier (300) is PLL lock signal (44),[1] whereas in Figure 2 of Applicants' specification the signal fed to the non-inverting input of Applicants' comparator (46) is a signal from a capacitor and resistor network used to measure a period of time that a synchronization signal is asserted. Accordingly, amplifier (300) does not constitute "a comparator that compares a first reference signal with a signal from [a] capacitor and resistor network used to measure the period of time that [a] synchronization signal is asserted," as presently claimed.

In light of the foregoing, claim 1, as amended, is submitted to be allowable over the cited art. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 1, and corresponding dependent claims 3, 4, 6-8.

[1] Although a capacitor (310) and resistors (306) and (308) are also connected to the non-inverting input of amplifier (300), these resistors and capacitor are not used to measure a period of time that a synchronization signal is asserted. For example, capacitor (310) is described as a "DC blocking capacitor." *See Lutz* at col. 7, lines 49 and 50.

B. Independent Claim 9

Claim 9, as amended, recites a fiber-optic transponder comprising, among other things, a translation circuit including:

> a level detector that compares [a] synchronization signal with a first reference signal to produce a logical signal based on the comparison;
>
> a timer adapted to measure a period of time that the logical signal is asserted to produce a timer signal; and
>
> a comparator that compares the timer signal with a second reference signal to produce a lock signal for use by the host device,

Figure 2 of Applicants' specification (copied below) illustrates an example embodiment of the claimed translation circuit including a level detector (40), a timer (including, e.g., capacitor (44) and resistor (R4)), and a comparator (46).

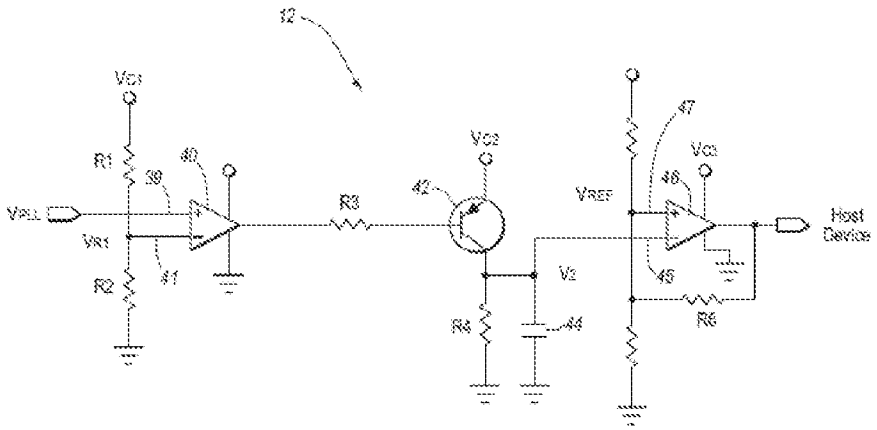


Fig. 2

In rejecting claim 9, the Examiner relies on *Khoury* as purportedly teaching certain elements of claim 9, but concedes that *Khoury* "fails to disclose the limitations of the PLL." *See Office Action* at 6. The Examiner instead cites *Lutz* for its purported teaching of a PLL and a translation circuit. *See id.* However, as explained below, the "translation circuit" of *Lutz* does not include the claimed "comparator."

In the Office Action, the Examiner characterizes amplifier (300) within lock detector and timer (16) as corresponding to a "level detector that compares the synchronization signal with a reference signal and produces logical signals." *See Office Action* at 8. Moreover, the Examiner characterizes lock detector and timer (16) and timer (18) as corresponding to a "timer adapted to measure a period of time that the synchronization signal is asserted." *See id.* However, the Examiner has not identified "a comparator that compares the timer signal with a second reference signal and outputs a lock signal for use by the host device based on the comparison." For example, amplifier (300) does not appear to correspond to the claimed comparator because the Examiner identifies it as corresponding to the claimed "level detector." Moreover, none of the circuitry in timer (18) appears to correspond to the claimed comparator because the Examiner identifies time (18) as corresponding to the claimed "timer."

In light of the foregoing, claim 9, as amended, is submitted to be allowable over the cited art. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 9, and corresponding dependent claims 13 and 29.

C. Independent Claim 14

Claim 14, as amended, recites a method comprising, among other things:

> obtaining an average of the synchronization signal over a period of time; [and]
>
> comparing the average of the synchronization signal with a reference signal to determine whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency.

Figure 4 of Applicants' specification (copied below) illustrates an example embodiment of circuitry configured to implement the method of claim 14. For example, as discussed in Applicants' specification, the circuitry uses a capacitor (76) to obtain an average of a synchronization signal (V_{PLL}) over a period of time and uses a comparator (70) to compare the average with a references signal (V_{REF}). *See* Applicants' specification at ¶¶ 39 and 40.

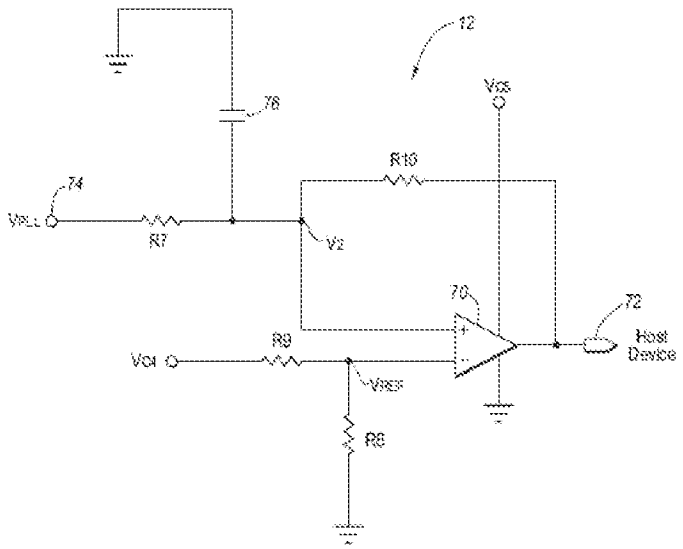


Fig. 4

In contrast, the cited art, whether considered individually or in combination, fails to teach or suggest the foregoing limitations.

According to the Examiner, a voltage across a capacitor (360) in *Lutz's* timer (18) "would be an average of [a] synchronization signal over a period of time." *See Office Action* at 11. Applicants respectfully disagree because capacitor (360) is not coupled to receive the lock signal on line (44), which the Examiner identified as corresponding to the claimed "synchronization signal." *See Office Action* at 8. Nonetheless, even assuming, for sake of argument, the voltage across capacitor (360) can be considered an average of a synchronization signal over a period of time, the voltage across capacitor (360) is not "compared…with a reference signal to determine whether the synchronization signal is caused by the phase locked loop locking onto a data signal or by the phase locked loop passing a hunting frequency through a data signal frequency," as presently claimed.

In light of the foregoing, claim 14, as amended, is submitted to be allowable over the cited art. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 14, and corresponding dependent claim 18. New claim 30 also depends from claim 14 and is submitted to be in condition for allowance at least by virtue of its dependence from allowable claim 14.

D. Independent Claim 19

Claim 19 recites, among other things, "a timing circuit adapted to measure a period of time that the synchronization signal is asserted using at least a capacitor arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted." The Examiner first identified a capacitor (318) in *Lutz* as the claimed capacitor. *See Office Action* at 8 and 9 (citing *Lutz* at column 8, lines 19-22). However, the Examiner later identified a different capacitor (360) in *Lutz* as the claimed capacitor that is "arranged to discharge when the synchronization signal is asserted and to charge when the synchronization signal is not asserted." *See id.* (citing *Lutz* at column 8, lines 55-67, which refers to "discharge capacitor 360"). Both capacitors cannot logically correspond to the claimed "**a** capacitor."

In fact, capacitor (318) is part of a first timer (16) that "develop[s] on a line 46 a (stabilization signal) of predetermined period after [a] lock signal has stabilized," whereas capacitor (360) is part of a second timer (18) that "responds to the delayed lock signal developed on line 46…[and] causes the state of [a] reset signal to change and, a predetermined time thereafter, it causes the state of [a] latch signal to change." *See Lutz* at col. 3, line 56, through col. 4, line 2, and Figure 1. Therefore, the capacitors are used in different timers for different purposes and are not both used by a single timing circuit (or timer) to "measure a period of time that the synchronization signal is asserted," as claimed.

Applicants respectfully note that while the foregoing points with respect to claim 19 were raised in Applicants previous response, the Examiner has failed to take note of and address these points, contrary to MPEP guidance.

In light of the foregoing, Applicants respectfully submit that no *prima facie* case of anticipation has been established with respect to claim 19. Accordingly, Applicants respectfully request withdrawal of the rejection of claim 19, and corresponding dependent claims 20-24, 26, and 28.

II. Charge Authorization

The Commissioner is hereby authorized to charge payment of any of the following fees that may be applicable to this communication, or credit any overpayment, to Deposit Account

No. 23-3178: (1) any filing fees required under 37 CFR § 1.16; (2) any patent application and reexamination processing fees under 37 CFR § 1.17; and/or (3) any post issuance fees under 37 CFR § 1.20. In addition, if any additional extension of time is required, which has not otherwise been requested, please consider this a petition therefor and charge any additional fees that may be required to Deposit Account No. 23-3178.

CONCLUSION

In view of the foregoing, Applicants submit that the pending claims are allowable. In the event that Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview or overcome by an Examiner's Amendment, Examiner is requested to contact the undersigned attorney.

Dated this 25th day of May 2010.

Respectfully submitted,

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